

**REMARKS**

The amendment to claim 1 incorporates the limitation of original claim 3. Applicants submit that the amendment does not add any new matter to the disclosure or raise any new issues and that it simplifies the issues for appeal. Applicants respectfully request that the amendment be entered.

The invention centers on methods of forming sub-50nm pitch features using lithography. The invention is characterized by the use of resist having low activation energy acid labile protecting groups (specifically, ketals, acetals and orthoesters) and by the use of a controlled low temperature post-exposure treatment (temperature and time combination). This combination allows for the creation of such fine features while avoiding blur.

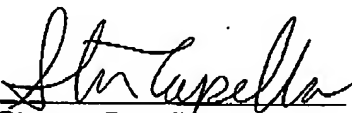
Varanasi et al. (US 2003/0182534 A 1) discloses a process using photoresist which may contain low activation energy protecting groups. Varanasi et al. uses a conventional post-exposure bake step of involving treatment at 100°C or greater. While Varanasi et al. references a feature size of 130nm or less, the smallest feature size actually resolved in Varanasi et al. is on the order of 150nm. Varanasi et al. does not disclose or suggest the claimed combination of using a photoresist of low activation energy and mild post-exposure treatment presently claimed, nor the results associated with such combination, namely the ability to resolve features at 50 nm half pitch.

Yamada et al. (US 6,399,273) discloses specific photoresists which are thermally treated prior to exposure where the photoresists have improved etch resistance. Yamada discloses a lithography process using a post-exposure bake condition of at least about 60°C, more preferably at least about 100°C. The temperatures actually used in the examples of Yamada et al. are at least 120°C.

The features resolved in the examples of Yamada et al. are on the order of 1000 nm. Further, applicants submit that the temperatures actually used by Yamada et al. correspond to those normally used in the art. Thus, one of ordinary skill would not consider Yamada et al. as providing any special instruction regarding post-exposure bake conditions, much less that one would be able to use the unconventional conditions of the invention as part of a combination of process features which enable sub-50nm pitch resolution. Thus, applicants submit that the combination of Yamada et al. with Varanasi et al. would still result in the use of a post-exposure treatment at temperatures exceeding the claimed range. The combination of Yamada et al. with Varanasi et al. would still fail to disclose or suggest the claimed combination of using a photoresist of low activation energy and mild post-exposure treatment, nor the results associated with such combination, namely the ability to resolve features at 50nm half pitch.

For the above reasons, applicants submit that the claims of the present application are now in condition for allowance. Such allowance is earnestly and respectfully solicited.

Respectfully submitted,  
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